DATA SHEET

SDN8000G
80-Common Dot-matrix STN LCD Driver

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1 GENERAL

1.1 Description

The SDN8000G is an 80-common dot-matrix STN LCD driver. It is designed to be paired with the SDN0080G 80-segment driver.

1.2 Features

- 80-output common driver for dot-matrix STN LCD.
- Display duty : 1/64 to 1/256
- Power-down mode for reducing power consumption.
- External LCD bias voltage.
- Capability of being cascaded in application to expand common number.
- Support single mode operation (80-bit shift register) and dual mode operation (40-bit x 2 shift register).
- In single mode operation, shift direction can be: O1 → O80 or O80 → O1.
- In dual mode operation, shift direction can be: O1 → O40 and O41 → O80, or O80 → O41 and O40 → O1.
- Operating voltage range (control logic): 2.7 ~ 5.5 volts.
- Operating voltage range (high voltage, V_{DD}-V_{EE}): 12 ~ 32 volts.
- Data transfer clock: 6.0 MHz, when V_{DD}= 5 volts.
- Operating temperature range: -20 to +75 °C.
- Storage temperature range: -40 to +125 °C.

1.3 Ordering information

Table 1 Ordering information

TYPE NUMBER	DESCRIPTION
SDN8000G-LQFPG	LQFP100 Green package.
SDN8000G-QFPG	QFP100 Green package.
SDN8000G-LQFP	LQFP100 package.
SDN8000G-QFP	QFP100 package.
SDN8000G-D	tested die.

2 FUNCTIONAL BLOCK DIAGRAM AND DESCRIPTION

2.1 Functional block diagram

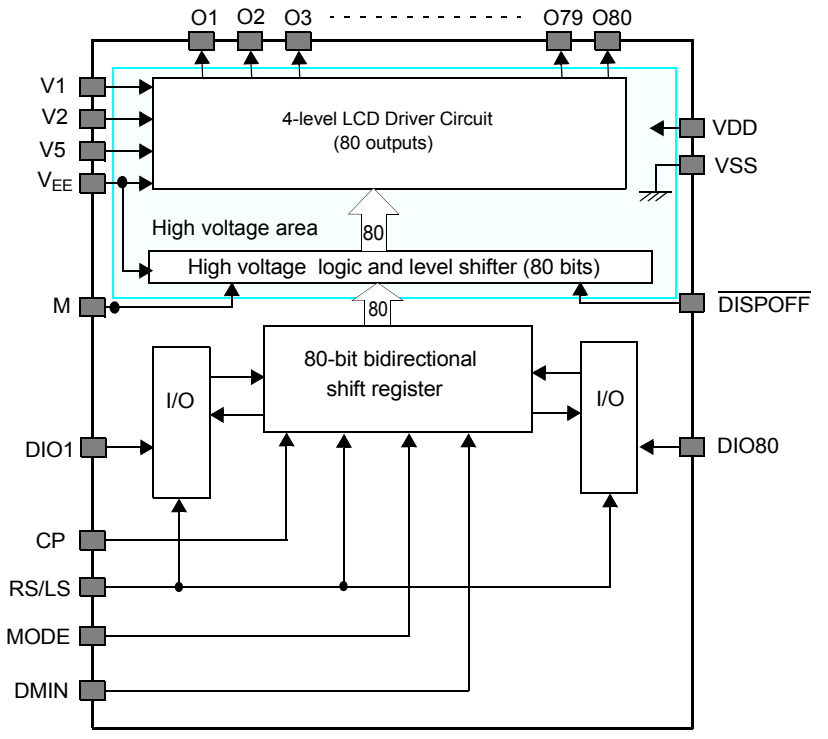


Fig.1 Functional Block Diagram

3 PINNING INFORMATION

3.1 Pinning diagram

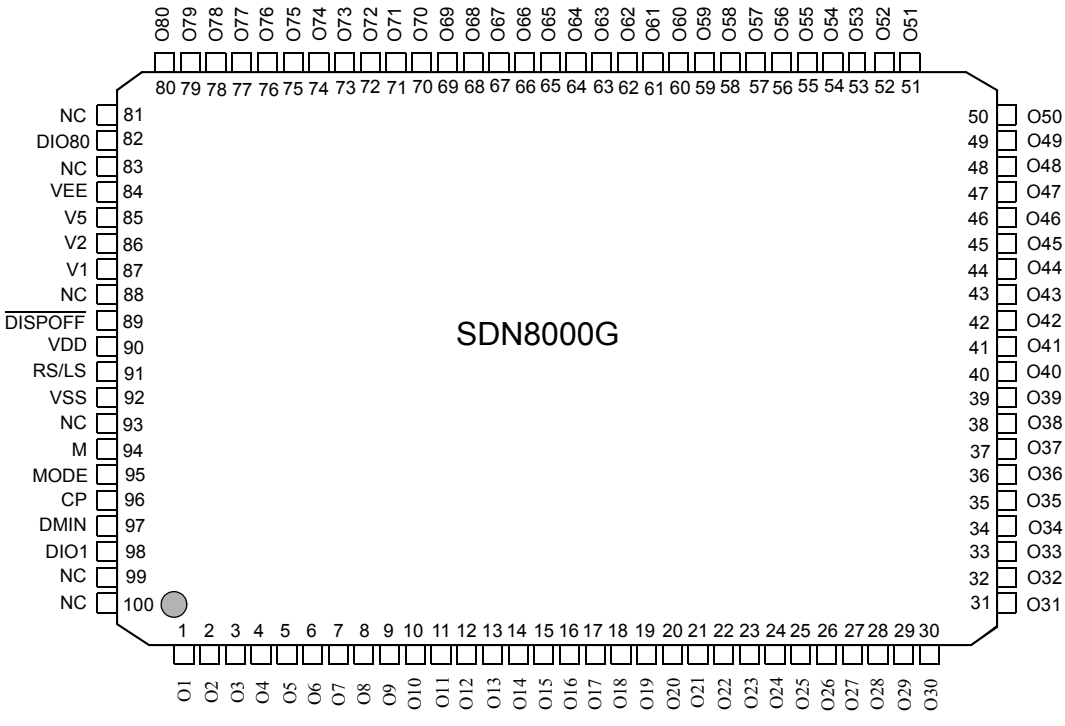


Fig.2 Pin diagram of QFP100 / LQFP100 package

3.2 Signal description

Table 2 Pin signal description.

To avoid a latch-up effect at power-on: $V_{SS} - 0.5\ V <$ voltage at any pin at any time $< V_{DD} + 0.5\ V$.

Pin number	SYMBOL	I/O	DESCRIPTION
1~80	O1~O80	Output	Common driver output. Please refer to Table 3 for output voltage level.
81, 83, 88, 93, 99, 100	NC	Input	No Connection. These pins are not used in application and should be left open.
82	DIO80	I/O	Data input/output pin for cascading application.
84, 85, 86, 87	V_{EE}, V5, V2, V1	Input	LCD bias voltage. V1 and V_{EE} are selected levels. V2 and V5 are unselected levels.
89	$\overline{\text{DISPOFF}}$	Input	Display Disable. When $\overline{\text{DISPOFF}}$=L, the outputs O1~O81 are all at a fixed level of V1. When $\overline{\text{DISPOFF}}$=H, the display can be turned ON.
90	VDD	Input	Power supply for control logic.
91	RS/LS	Input	Select shift direction of COMMON scan data from a controller. When RS/LS=L, right shift is selected. When RS/LS=H, left shift is selected. For detail, please also refer to Table 4, Mode selection.
92	VSS	Input	Ground.
94	M	Input	Frame signal, for alternating LCD bias voltage.
95	MODE	Input	Mode control. When MODE= LOW, single mode operation is selected. When MODE= HIGH, dual mode operation is selected. Please refer to Table 4, Mode selection.
96	CP	Input	Scan data latch clock.
97	DMIN	Input	Second data input for dual mode application. Please refer to Table 4, Mode selection.
98	DIO1	I/O	Data input/output pin for cascading application.

4 FUNCTIONAL DESCRIPTION

4.1 Common output drive (O1~O80)

The voltage level of the outputs O1~O80 is determined by input data (scan data), M (frame signal), and $\overline{\text{DISPOFF}}$, as given in the following table.

Table 3 output voltage level of O1~O80

M	Data	$\overline{\text{DISPOFF}}$	Output
L	L	H	V2
L	H	H	V_{EE}
H	L	H	V5
H	H	H	V1
X	X	L	V1

In the above table, X= don't care and must be tied either to H or L.

4.2 Mode selection

The mode selection and scan data shift direction is given in the following table.

Table 4 Mode selection

Mode pin	**RS/LS pin**	**Data transfer direction**	**DIO1**	**DIO80**	**DMIN**
L (Single mode)	LOW (right shift)	O1 → O80	IN	OUT	X
	HIGH (left shift)	O80 → O1	OUT	IN	X
H (Dual mode)	LOW (right shift)	O1 → O40 O41 → O80	IN	OUT	IN
	HIGH (left shift)	O80 → O41 O40 → O1	OUT	IN	IN

Note: X= don't care. It can be tied either to VDD or to VSS.

4.3 Cascading connection

4.3.1 SINGLE MODE, RIGHT SHIFT

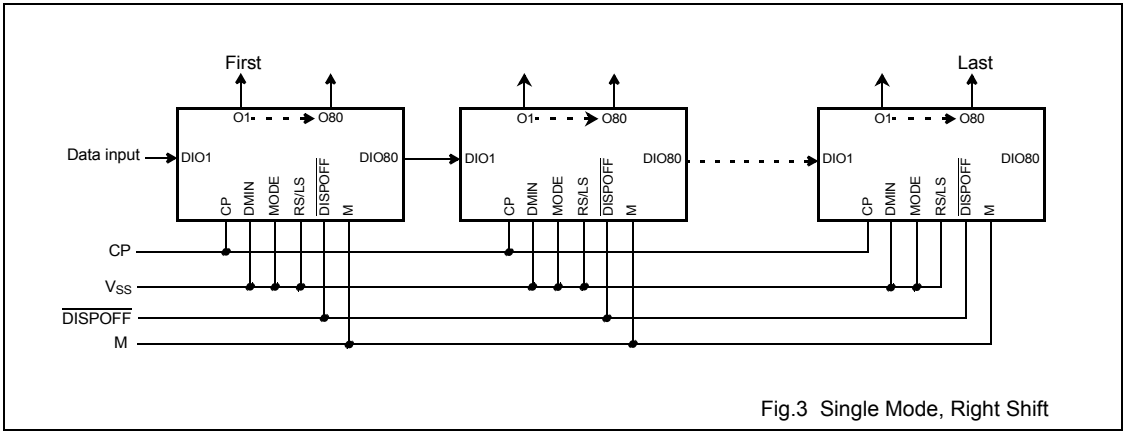


Fig.3 Single Mode, Right Shift

4.3.2 SINGLE MODE, LEFT SHIFT

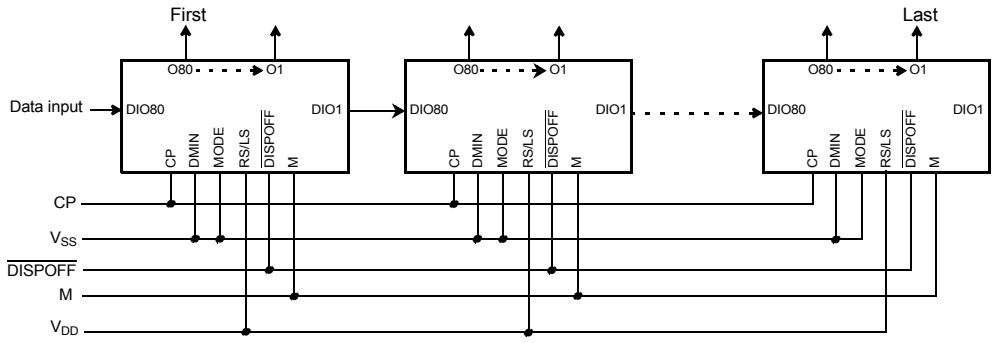


Fig.4 Single Mode, Left Shift

4.3.3 DUAL MODE, RIGHT SHIFT

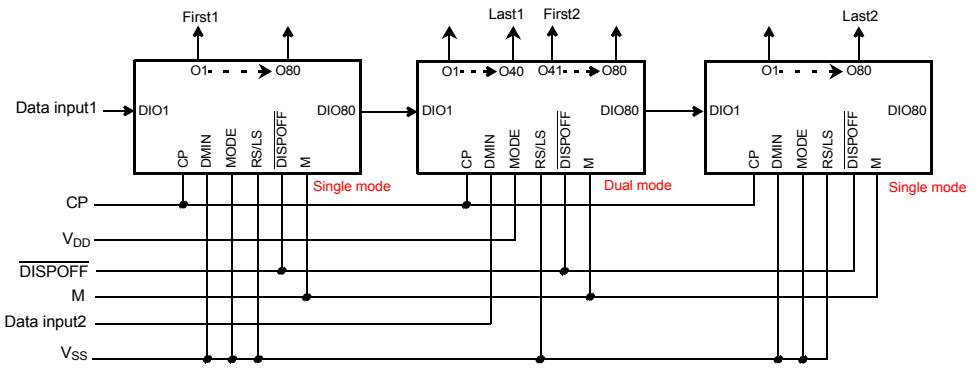


Fig.5 Dual Mode, Right Shift

4.3.4 DUAL MODE, LEFT SHIFT

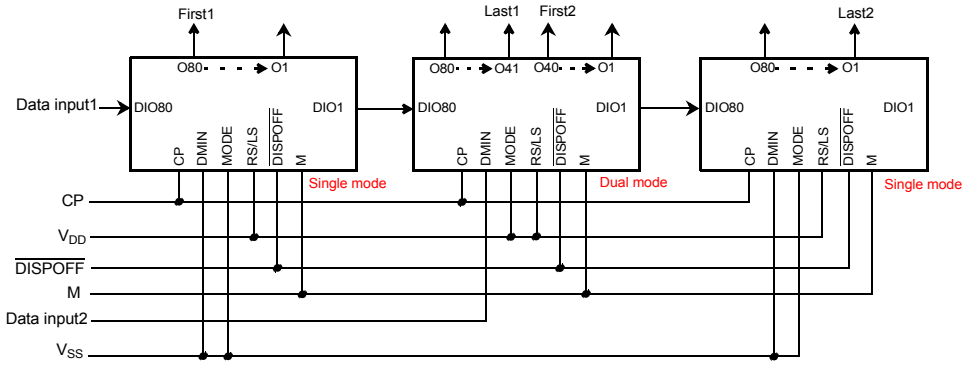


Fig.6 Dual Mode, Left Shift

5 ABSOLUTE MAXIMUM RATING

Table 5 Absolute maximum rating

V_{DD} = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS} unless otherwise specified; T_{amb} = 25±2°C.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	Voltage on the V_{DD} input	−0.3	+7.0	V
V_{DD}-V_{EE}	LCD bias voltage, note 1	0	35	V
Vi(max)	Maximum input voltage to input pins	-0.3	V_{DD} + 0.3	
T_{amb}	Operating ambient temperature range	-20	+ 75	°C
T_{stg}	Storage temperature range	−40	+125	°C

Note:

1. The following conditions must always be met: $V_{DD} \geq V1 > V2 > V5 > V_{EE}$, V_{DD}-V2 ≤ 7V, and V5-V_{EE}≤ 7V.

6 DC CHARACTERISTICS

Table 6 DC Characteristics

V_{DD} = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS} unless otherwise specified; T_{amb} = 25±2 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply voltage for control logic	Please refer to Fig. 9 for DC power-up sequence.	2.7	5.0	5.5	V
V_{DD}-V_{EE}	LCD bias voltage	Note 1.	12		32	
V_{IL}	Input LOW voltage of input pins	DIO1, DIO80, CP, M, DMIN,MODE, RS/LS, DISPOFF	0		0.2V_{DD}	V
V_{IH}	Input HIGH voltage of input pins	DIO1, DIO80, CP, M, DMIN,MODE, RS/LS, DISPOFF	0.8V_{DD}		V_{DD}	V
I_{IL}	Input LOW leakage current of input pins (i. e. Reverse leakage current of input ESD protection diode)	V_{IN}=V_{SS}, DIO1, DIO80, CP, M, DMIN,MODE, RS/LS, DISPOFF			1	μA
I_{IH}	Input HIGH leakage current of input pins (i. e. Reverse leakage current of input protection diode)	V_{IN}=V_{DD}, DIO1, DIO80, CP, M, DMIN,MODE, RS/LS, DISPOFF			1	μA
V_{OL}	Output LOW voltage level of the DIO1 and DIO80 pins	I_{OL}=400μA	0.0		0.4	V
V_{OH}	Output HIGH voltage level of the DIO1 and DIO80 pins	I_{OH}=-400μA	V_{DD} − 0.4		V_{DD}	V
I_{STBY}	Stand-by current	Note 2.			2	μA
I_{SS}	Operating current	Note 3.			80	μA
I_{EE}	Operating current	Note 4.			80	μA
Ci	Input capacitance of the CP pin	The CP clock frequency is 1 MHz.		5.0		pF
R_{ON1}	Driver ON resistance at V_{LCD}= 30 V	Note 5.			1.0	KΩ
R_{ON2}	Driver ON resistance at V_{LCD}= 20 V	Note 6.			1.0	KΩ

Notes:

1. The following conditions: $V_{DD} \geq V1 > V2 > V5 > V_{EE}$, V_{DD}-V2 ≤ 7V, and V5-V_{EE}≤ 7V must always be met.
2. V_{DD}-V_{EE}=30 V, CP=LOW, Output unloaded; measured at the V_{SS} pin.
3. Condition for the measurement: V_{LCD}=V_{DD}-V_{EE}=30 V, V_{DD}=5.5 V, CP=14 KHz, No load. This is the current flowing from V_{DD} to V_{SS}, measured at the V_{SS} pin.
4. Condition for the measurement: V_{LCD}=V_{DD}-V_{EE}=30 V, V_{DD}=5.5 V, CP=14 KHz, No load. This is the current flowing from V_{DD} to V_{EE}, measured at the V_{EE} pin.
5. Condition for the measurement: V_{DD}-V_{EE}=30 V, $|V_{DE}-V_O|$=0.5 V, where V_{DE}= one of V1, V2, V5, or V_{EE}. V1=V_{DD}, V2= (16/17) x (V_{DD}-V_{EE}), V5= (1/17) x (V_{DD}-V_{EE}). For the driver circuits (O1~O80), please refer to Section 9, Pin Circuits.

6. Condition for the measurement: V_{DD}-V_{EE}=20 V, |V_{DE}-V_O|=0.5 V, where V_{DE}= one of V1, V2, V5, or V_{EE}. V1=V_{DD}, V2= (16/17) x (V_{DD}-V_{EE}), V5= (1/17) (V_{DD}-V_{EE}). For the driver circuits (O1~O80), please refer to Section 9, Pin Circuits.

7 AC CHARACTERISTICS

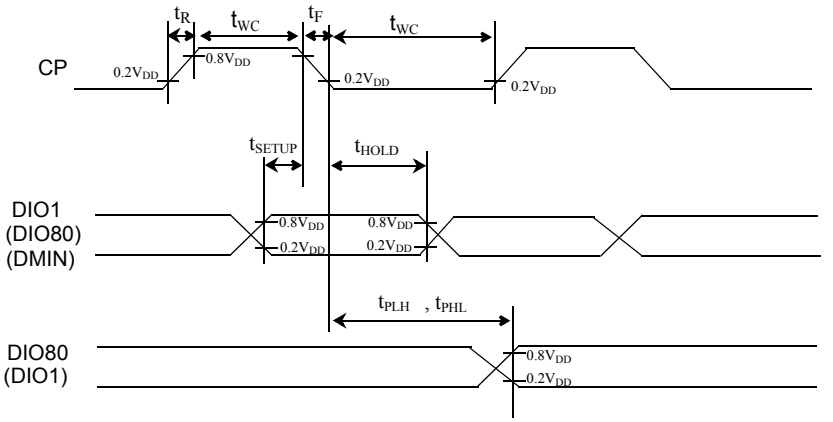


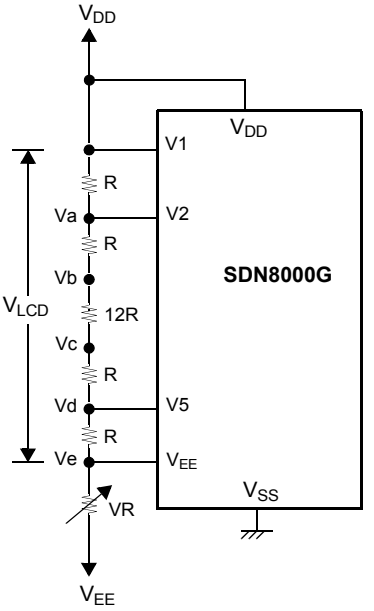
Fig.7 AC characteristics

Table 7 AC Characteristics

V_{DD} = 5 V ±10%; V_{SS} = 0 V; all voltages with respect to V_{SS} unless otherwise specified; T_{amb} = 25 ±2 °C.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
f_{CP}	CP clock frequency			1.0	MHz
T_{WC}	CP clock pulse width		62		ns
t_{SETUP}	Input data setup time	Data change of DIO1, DIO80, and DMIN to the falling edge of the CP clock.	100		ns
t_{HOLD}	Input data hold time.	Falling edge of the CP clock to the data change of DIO1, DIO80, and DMIN.	100		ns
t_R	CP rise time			50	ns
t_F	CP fall time			50	ns
t_{PLH} ,t_{PHL}	Output delay time	CP→DIO1, CP→DIO80, Load=15pF.		250	ns

8 LCD BIAS VOLTAGE



$Va = V_{DD} - (1/16)\ V_{LCD}$

$Vb = V_{DD} - (2/16)\ V_{LCD}$

$Vc = V_{DD} - (14/16)\ V_{LCD}$

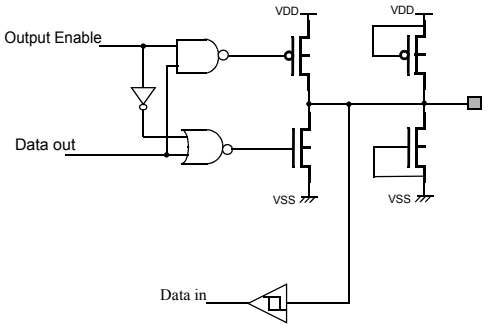
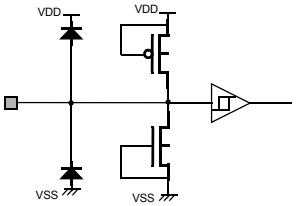
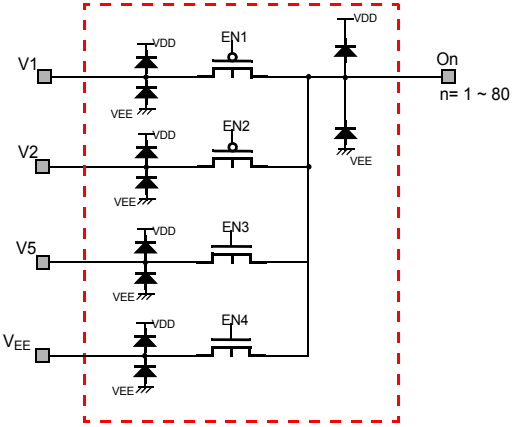
$Vd = V_{DD} - (15/16)\ V_{LCD}$

$Ve = V_{DD} - (16/16)\ V_{LCD}$

Fig.8 LCD bias voltage

9 PIN CIRCUITS

Table 8 MOS-level schematics of all input, output, and I/O pins.

SYMBOL	Input/ output	CIRCUIT	NOTES
DIO1, DIO80	I/O		
CP, RS/LS, M, MODE, DMIN, $\overline{\text{DISPOFF}}$	Inputs		
O1~O80, V1, V2, V5, V_{EE}	Driver outputs, High voltage inputs		

10 APPLICATION NOTES

1. It is recommended that the following power-up sequence be followed to ensure reliable operation of your display system. As the ICs are fabricated in CMOS and there is intrinsic latch-up problem associated with any CMOS devices, proper power-up sequence can reduce the danger of triggering latch-up. When powering up the system, control logic power must be powered on first. When powering down the system, control logic must be shut off later than or at the same time with the LCD bias (V_{EE}).

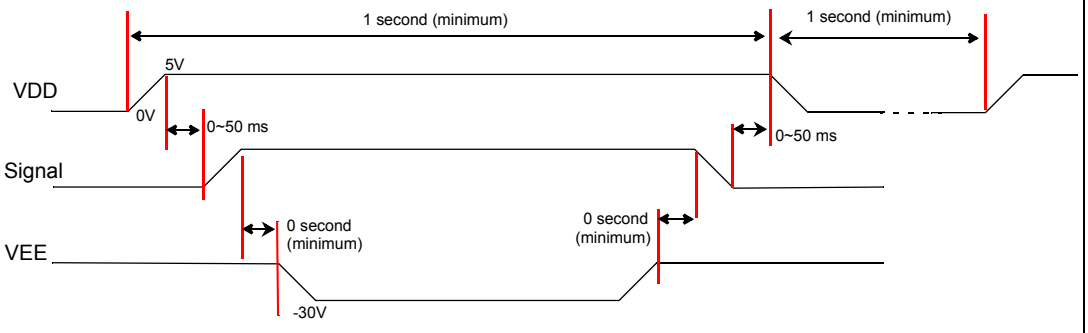
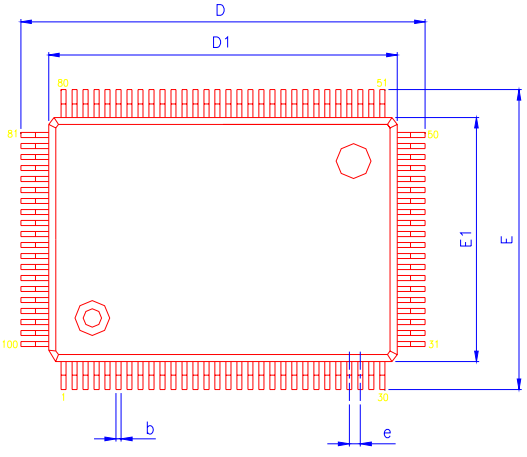
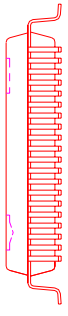


Fig.9 Recommended power up/down sequence

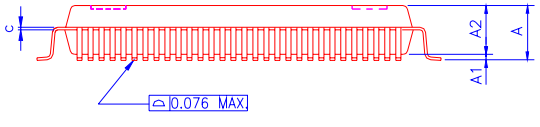
11 PACKAGE INFORMATION

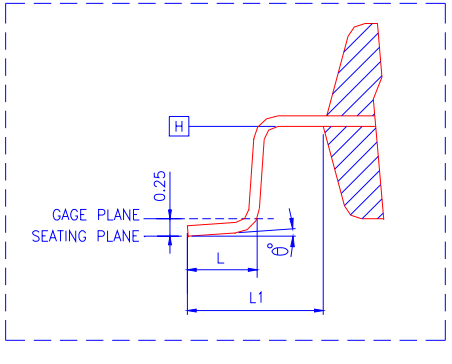




SYMBOLS	MIN.	NOM	MAX.
A	–	–	3.40
A1	0.25	–	0.50
A2	2.50	2.70	2.90
b	0.22	–	0.40
c	0.11	–	0.23
D		23.20 BASIC	
D1		20.00 BASIC	
e		0.65 BASIC	
E		17.20 BASIC	
E1		14.00 BASIC	
L	0.73	0.88	1.03
L1	–	1.60	–
θ°	0	–	7

UNIT : mm





NOTES:
1.JEDEC OUTLINE:MS-022 GC-1

2.DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.

3.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.

4.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION .

SDN8000G
QFP100 Package Outline Drawing

12 SOLDERING

12.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. For more in-depth account of soldering ICs, please refer to dedicated reference materials.

12.2 Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, please contact Avant for drypack information.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

12.3 Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

12.4 Repairing soldered joints

Fix the component by first soldering two diagonally- opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

13 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Avant customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Avant for any damages resulting from such improper use or sale.